# APPLICATION UNDER UNITED STATES PATENT LAWS

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Invention: METHOD AND SYSTEM TO ENHANCE THE REMOVAL OF HIGH-K DIELECTRIC MATERIALS

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## SPECIFICATION

## Title of the Invention

A Method and System to Enhance the Removal of High-k Dielectric Materials

**[0001]** This application is based on and claims the benefit of United States Provisional Application Number 60/406,031, filed August 27, 2002, the entire contents of which are incorporated herein by reference.

## Field of the Invention

**[0002]** The present invention is related to removal of materials from a substrate, particularly to removal of high-k dielectric layers from a semiconductor substrate.

## Background of the Invention

**[0003]** In the semiconductor industry, the minimum feature sizes of microelectronic devices are approaching the deep sub-micron regime to meet the demand for faster, lower power microprocessors and digital circuits. Process development and integration issues are key challenges for new gate stack materials and silicide processing, with the imminent replacement of $SiO_2$ and Si-oxynitride ($SiN_xO_y$) with high-permittivity dielectric materials (also referred to herein as "high-k" materials), and the use of alternative gate electrode materials to replace doped poly-Si in sub-0.1 μm complementary metal-oxide semiconductor (CMOS) technology.

**[0004]** Dielectric materials featuring a dielectric constant greater than that of $SiO_2$ (k~3.9) are commonly referred to as high-k materials. In addition, high-k materials may refer to dielectric materials that are deposited onto substrates (e.g., $HfO_2$, $ZrO_2$) rather than grown on the surface of the substrate (e.g., $SiO_2$, $SiN_xO_y$). High-k materials may incorporate metallic silicates or oxides (e.g., $Ta_2O_5$ (k~26), $TiO_2$ (k~80), $ZrO_2$ (k~25), $Al_2O_3$ (k~9), HfSiO, $HfO_2$ (k~25)). During the manufacturing of semiconductor devices, the high-k layers must be etched and removed in order to allow silicidation for the

source/drain regions, and to reduce the risk of metallic impurities being implanted into the source/drain regions during ion implantation.

## Summary of the Invention

**[0005]** The present invention relates to a plasma process to modify a high-k dielectric layer through exposure of the high-k layer to the plasma, resulting in a modified layer that etches efficiently using wet etch processes.

**[0006]** The plasma process can comprise an inert gas and/or a reactive gas mixture, and the process can be implemented in-situ, as an additional step performed at the end of a gate-electrode etching process, or as an additional step added at the end of a spacer-etch process.

## Brief Description of the Drawings

**[0007]** A more complete appreciation of the invention and many of the attendant advantages thereof will become readily apparent with reference to the following detailed description, particularly when considered in conjunction with the accompanying drawings, in which:

**[0008]** FIG. 1 shows a flowchart illustrating a method of modifying a layer of high-k material according to the present invention;

**[0009]** FIGS. 2a-2c show a schematic cross-sectional representation of the steps of modifying and removing a layer high-k dielectric material according to the present invention;

**[0010]** FIG. 3 shows a plasma processing system according to a preferred embodiment of the present invention;

**[0011]** FIG. 4 shows a plasma processing system according to an alternate embodiment of the present invention;

**[0012]** FIG. 5 shows a plasma processing system according to an alternate embodiment of the present invention;

**[0013]** FIG. 5A shows a plasma processing system according to an alternate embodiment of the present invention;

**[0014]** FIG. 5B shows a plasma processing system according to an alternate embodiment of the present invention;

**[0015]** FIG. 6 shows a plasma processing system according to an alternate embodiment of the present invention;

**[0016]** FIG. 6A shows a plasma processing system according to an alternate embodiment of the present invention;

**[0017]** FIG. 6B shows a plasma processing system according to an alternate embodiment of the present invention; and

**[0018]** FIG. 7 shows a flowchart illustrating wet etching of a modified layer of high-k material.

## Detailed Description of the Embodiments

**[0019]** In one embodiment of the invention, a plasma processing system uses an inert gas to modify a high-k dielectric layer by exposure to the plasma region. The inert gas species in the process gas can be selected from the group of noble gases He, Ne, Ar, Kr, and Xe, or other gases that are non-reactive towards a high-k layer in a plasma environment. The gas-phase plasma ions bombard and modify the high-k layer, but the ions are physically prevented from attacking the underlying Si layer by the high-k layer. In a separate wet etch step following the plasma process, the plasma modified high-k layers etch faster than high-k layers that were not subject to the plasma treatment.

**[0020]** In an alternate embodiment, the disclosed plasma treatment employs a reactive plasma that chemically reacts with the high-k layer, and the ions have sufficient energy to effectively disrupt and/or thin the high-k layer so that a wet etching process is able to efficiently remove the disrupted (modified) high-k layer. When a reactive plasma is used to modify the high-k layer, the process gas and plasma conditions are selected such that the patterned gate-conductor features and other materials may not be etched or damaged. For example, the process gas can comprise HBr or HCl, and an inert gas such as He.

**[0021]** In a patterned etch process, where fine features are defined by a photoresist or a hard mask, the modification of the exposed high-k layer is substantially anisotropic due to ion bombardment that is parallel to the surface normal. As a result, the increase in the wet etch rate of the modified high-k layer is anisotropic. In other words, the result of the plasma modification of the high-k layer and the following wet etch step is anisotropic etching and removal of the exposed high-k layer.

**[0022]** In the manufacturing of semiconductor devices, the plasma treatment of the high-k layer gas according to the present invention can be carried out at different stages during the patterning process. For example, the plasma treatment can be added to the end of a normal gate etch process recipe, or added to a standard spacer-etch process.

**[0023]** For example, a sequence for forming a gate electrode that is defined by a hard mask can comprise: 1) "break-through", that etches through the hard mask; 2) "main-etch", that forms the electrode features; and 3) "over-etch", that etches and removes the (high-k) dielectric layer overlying the Si substrate. Etch step 3) that removes the high-k layer, frequently involves the use aggressive halogen containing precursors that have very low selectivity towards etching Si. These precursors (e.g., $CF_4$ or HBr in the presence of $O_2$) often necessitate the use of elevated substrate temperature to increase the volatility of the etch byproducts and the use of these precursors may furthermore require a large physical etch component and polymer formation to achieve adequate etch selectivity. The increased temperatures, in turn, can force a move from photoresist masking to hard masks. Consequently, there is a risk of damaging the underlying Si layer if the etch process is not promptly terminated when the high-k layer has been removed.

**[0024]** The above plasma etch step 3) can be replaced by a plasma modifying/thinning step, where the ions in the plasma bombard and modify the high-k layer without completely removing it. In a reactive plasma process, the processing gas can comprise HBr or HCl, and an inert gas. The wet etch process can comprise hot sulfuric acid, resulting in removal of the high-k layer by a standard wet clean process. Since the high-k layer is not traversed during the modifying/thinning step, the likelihood of damage occurring to the

underlying Si layer is reduced. If the thinning step is carried out for too long, the high-k layer is traversed, resulting in damage to the underlying Si layer.

**[0025]** The exact effect of the plasma treatment on the high-k layer is currently not known. However, the plasma treatment may increase the amorphous content of the high-k layer and possibly breaks chemical bonds that create atomic fragments in the high-k layer. In addition to using inert gases the disclosed plasma treatment can utilize reactive gases, where the ion energy is adequate to disrupt the atomic structure of the high-k layer in such a way that the subsequent wet-etching process is able to remove the modified high-k layer. When using a reactive plasma, the process conditions can be selected such that the existing gate-conductor features are not etched.

**[0026]** The plasma treatment of the high-k layer can be incorporated into manufacturing of semiconductor devices by carrying out the plasma treatment at the end of the spacer-etch process. Sidewall spacers are used to achieve isolation between the gate and source/drain regions, as well as to facilitate fabrication of self-aligned, drain-engineered dopant structures. Sometimes, it is desirable to have the high-k layer remaining on the source/drain region while performing the spacer-etch process, so that the plasma environment is exposed to the "sacrificial" high-k material instead of the Si. After the spacer is formed, plasma treatment of the high-k layer according to the current invention is performed in-situ to modify the high-k layer and facilitate fast wet etching of the high-k layer.

**[0027]** The additional plasma treatment step can be added onto the end of the gate-electrode etching process, or the additional plasma treatment step can be added onto the end of the spacer-etch process. Advantageously, the invention can be performed in a separate process chamber or on a separate plasma etch tool.

**[0028]** After the plasma etch step, the wafer can be wet- etched using standard wet etching methods to remove the high-k layer. Then an ion implant process step forms the source/drain regions without the presence of a high-k layer on the silicon surface, which alleviates the risk of a knock-on implantation of impurities from the high-k layer into the source/drain regions. An additional benefit is that the high-k removal will not inhibit the silicidation of

the source/drain regions, a process step that is extremely sensitive to interfacial silicon surface layers.

**[0029]** Modification of high-k materials using phosphorous ion implantation, has shown significant increase in wet etch rates of the ion implanted high-k material. However, this requires the incident ion kinetic energy to be significantly reduced from the normal implant kinetic energy. This can be explained through the reduced collision cross-section coupled with the increased wafer surface temperature by high kinetic energy ions. In other words, ions with kinetic energy in the range of a standard ion-implant process have much reduced collision cross section with the high-k layer, and as a result, the incident ions simply pass through the thin (e.g., 3nm to 5nm) high-k layers without causing significant bond-breaking collisions. Also, high-energy implants heat up the wafer and the increased wafer temperature can anneal and repair the broken bonds and thereby significantly restore the initial properties of the high-k layer.

**[0030]** FIG. 1 shows a flowchart illustrating a method of modifying a layer of high-k material according to the present invention. The method uses a plasma process to modify the high-k layer for the following wet etch process that removes the modified high-k layer from the substrate. In step 100, the process is started. In step 102, a layer is provided having a high-k material overlying a substrate, and the substrate is positioned in a plasma processing chamber. In step 104, a process gas comprising an inert gas and/or a reactive gas is introduced into the plasma processing chamber, and a plasma is started. In step 106, the layer of high-k material is exposed to the plasma, and the layer is modified due to ion bombardment in the plasma. When the process in step 106 has been carried out for the desired amount of time to modify the high-k layer, the process is ended in step 108.

**[0031]** FIGS. 2a-2c show a schematic cross-sectional representation of the steps of modifying and removing a layer high-k dielectric material. FIG. 2a shows a partially completed structure 200 comprising a high-k dielectric layer 204 overlying a semiconductor substrate 202, etched gate electrode features 206 and hard mask or photoresist layer 208 defining the patterned structure. FIG. 2b shows the partially completed structure 200 from FIG. 2a following a

plasma etch process. A modified high-k layer 210 is formed on the horizontal surface that is exposed to the plasma. The structure 200 in FIG. 2b is further processed using standard wet cleaning methods that are well known in the art to form the structure 200 in FIG. 2c where the modified high-k layer and the hard mask (or photoresist layer) have been removed and the structure is ready for further processing to form a semiconductor device.

**[0032]** Low selectivity of high-k dielectrics to $SiO_2$, can be problematic when attempting to clear high-k layers overlying Si and $SiO_2$ regions simultaneously. Over-etching high-k dielectrics can lead to excessive removal of $SiO_2$ from the isolation regions of a device. Therefore, integration of high-k dielectrics may require the use of new etch processes with high selectivity to $SiO_2$. The suggested disruption of the molecular structure of the high-k layers during exposure to the plasma allows for a greater choice of wet etch chemistries, that have high etch selectivity of high-k materials to Si and $SiO_2$.

**[0033]** FIG. 3 shows a plasma processing system according to a preferred embodiment of the present invention. In FIGS. 3-6, like reference numbers are used to indicate like elements throughout. A plasma processing system 1 that is capable of sustaining a plasma is depicted in FIG. 3, which includes a plasma process chamber 10 configured to facilitate the generation of plasma in processing region 45. The plasma processing system 1 further comprises a substrate holder 20, upon which a substrate 25 to be processed is affixed, and a gas injection system 40 for introducing process gases 42 to the plasma process chamber 10, and a vacuum pumping system 50. The gas injection system 40 allows independent control over the delivery of process gases to the process chamber from ex-situ gas sources.

**[0034]** An ionizable gas or mixture of gases is introduced via the gas injection system 40 and the process pressure is adjusted. For example, conroller 55 is used to control the vacuum pumping system 50 and gas injection system 40. Desirably, plasma is utilized to create materials specific to a predetermined materials process, and to aid either the deposition of material to a substrate 25 or the removal of material from the exposed surfaces of the substrate 25.

**[0035]** Substrate 25 is transferred into and out of chamber 10 through a slot valve (not shown) and chamber feed-through (not shown) via robotic substrate transfer system where it is received by substrate lift pins (not shown) housed within substrate holder 20 and mechanically translated by devices housed therein. Once the substrate 25 is received from the substrate transfer system, it is lowered to an upper surface of the substrate holder 20.

**[0036]** In an alternate embodiment, the substrate 25 is affixed to the substrate holder 20 via an electrostatic clamp (not shown). Furthermore, the substrate holder 20 further includes a cooling system including a re-circulating coolant flow that receives heat from the substrate holder 20 and transfers heat to a heat exchanger system (not shown), or when heating, transfers heat from the heat exchanger system. Moreover, gas may be delivered to the backside of the substrate to improve the gas-gap thermal conductance between the substrate 25 and the substrate holder 20. Such a system is utilized when temperature control of the substrate is required at elevated or reduced temperatures. For example, temperature control of the substrate may be useful at temperatures in excess of the steady-state temperature achieved due to a balance of the heat flux delivered to the substrate 25 from the plasma and the heat flux removed from substrate 25 by conduction to the substrate holder 20. In other embodiments, heating elements, such as resistive heating elements, or thermo-electric heaters/coolers are included.

**[0037]** In the embodiment, shown in FIG. 3, the substrate holder 20 can further serve as an electrode through which radio frequency (RF) power is coupled to plasma in the processing region 45. For example, the substrate holder 20 can be electrically biased at a RF voltage via the transmission of RF power from an RF generator 30 through an impedance match network 32 to the substrate holder 20. The RF bias serves to heat electrons and, thereby, form and maintain plasma. In this configuration, the system operates as a RIE reactor, wherein the chamber and upper gas injection electrode serve as ground surfaces. A typical frequency for the RF bias ranges from 1 MHz to 100 MHz and is preferably 13.56 MHz.

**[0038]** In an alternate embodiment, RF power can be applied to the substrate holder electrode at multiple frequencies. Furthermore, the

impedance match network 32 serves to maximize the transfer of RF power to plasma in processing chamber 10 by minimizing the reflected power. Match network topologies (e.g., L-type, $\pi$–type, T-type) and automatic control methods are known in the art.

**[0039]** With continuing reference to FIG. 3, a process gas 42 is introduced to the processing region 45 through the gas injection system 40. Gas injection system 40 can include a showerhead, wherein the process gas 42 is supplied from a gas delivery system (not shown) to the processing region 45 through a gas injection plenum (not shown), a series of baffle plates (not shown) and a multi-orifice showerhead gas injection plate (not shown).

**[0040]** Vacuum pump system 50 can include a turbo-molecular vacuum pump (TMP) capable of a pumping speed up to 5000 liters per second (and greater), and a gate valve for throttling the chamber pressure. In conventional plasma processing devices utilized for dry plasma etch, a 1000 to 3000 liter per second TMP is employed. TMPs are useful for low pressure processing, typically less than 50 mTorr. For high pressure processing (i.e. greater than 100 mTorr), a mechanical booster pump and dry roughing pump are used.

**[0041]** A controller 55 includes a microprocessor, a memory, and a digital I/O port capable of generating control voltages sufficient to communicate and activate inputs to the plasma processing system 1 as well as monitor outputs from the plasma processing system 1. Moreover, the controller 55 is coupled to and exchanges information with the RF generator 30, the impedance match network 32, the gas injection system 40, plasma monitor system 57, and the vacuum pump system 50. A program stored in the memory is utilized to control the aforementioned components of a plasma processing system 1 according to a stored process recipe. One example of controller 55 is a digital signal processor (DSP); model number TMS320, available from Texas Instruments, Dallas, Texas.

**[0042]** The plasma monitor system 57 can comprise, for example, an optical emission spectroscopy (OES) system to measure excited particles in the plasma environment and/or a plasma diagnostic system, such as a Langmuir probe, for measuring plasma density. The plasma monitor system 57 can be used with controller 55 to determine the status of the etching process and

provide feedback to ensure process compliance. Alternately, plasma monitor system 57 can comprise a microwave and/or a RF diagnostic system.

**[0043]** FIG. 4 shows a plasma processing system according to an alternate embodiment of the present invention. The plasma processing system 1 of FIG. 4 further includes either a mechanically or electrically rotating DC magnetic field system 60, in order to potentially increase plasma density and/or improve plasma processing uniformity, in addition to those components described with reference to FIG. 3. Moreover, the controller 55 is coupled to the rotating magnetic field system 60 in order to regulate the speed of rotation and field strength.

**[0044]** FIG. 5 shows a plasma processing system according to an alternate embodiment of the present invention. The plasma processing system 1 of FIG. 5 further includes an upper plate electrode 70 to which RF power is coupled from an RF generator 72 through an impedance match network 74. A typical frequency for the application of RF power to the upper electrode ranges from 10 MHz to 200 MHz and is preferably 60 MHz. Additionally, a typical frequency for the application of power to the lower electrode ranges from 0.1 MHz to 30 MHz and is preferably 2 MHz. Moreover, the controller 55 is coupled to the RF generator 72 and the impedance match network 74 in order to control the application of RF power to the upper electrode 70.

**[0045]** FIG. 5A shows a plasma processing system according to an alternate embodiment of the present invention.The plasma processing system 1 in FIG. 5 is modified to contain a grounded lower electrode 20. In an alternate embodiment, a DC bias can be applied to the lower electrode 20.

**[0046]** FIG. 5B shows a plasma processing system according to an alternate embodiment of the present invention. The plasma processing system 1 in FIG. 5 is modified to contain a lower electrode 20 that is electrically isolated from the plasma processing system 1. In this setup, a floating potential can be formed on the lower electrode 20 and on the substrate 25 when the plasma is on.

**[0047]** FIG. 6 shows a plasma processing system according to an alternate embodiment of the present invention. The plasma processing system of FIG. 3 is modified to further include an inductive coil 80 to which RF power is

coupled via an RF generator 82 through an impedance match network 84. RF power is inductively coupled from the inductive coil 80 through a dielectric window (not shown) to the plasma-processing region 45. A typical frequency for the application of RF power to the inductive coil 80 ranges from 10 MHz to 100 MHz and is preferably 13.56 MHz. Similarly, a typical frequency for the application of power to the chuck electrode ranges from 0.1 MHz to 30 MHz and is preferably 13.56 MHz. In addition, a slotted Faraday shield (not shown) can be employed to reduce capacitive coupling between the inductive coil 80 and plasma. Moreover, the controller 55 is coupled to the RF generator 82 and the impedance match network 84 in order to control the application of power to the inductive coil 80.

**[0048]** In an alternate embodiment, the plasma is formed using electron cyclotron resonance (ECR). In yet another embodiment, the plasma is formed from the launching of a Helicon wave. In yet another embodiment, the plasma is formed from a propagating surface wave.

**[0049]** FIG. 6A shows a plasma processing system according to an alternate embodiment of the present invention. The plasma processing system of FIG. 6 is modified to contain a grounded chuck electrode 20. In an alternate embodiment, a DC bias can be applied to the chuck electrode 20.

**[0050]** FIG. 6B shows a plasma processing system according to an alternate embodiment of the present invention. The plasma processing system 1 of FIG. 6 is modified to contain a chuck electrode 20 that is electrically isolated from the plasma processing system 1. In this setup, a floating potential can be formed on the chuck electrode 20 and on the substrate 25 when the plasma is on.

**[0051]** FIG. 7 shows a flowchart illustrating wet etching of a modified layer of high-k material. In step 700 the process is started. In step 702, a modified layer of high-k material overlying a substrate is provided to a wet etch system. In step 704 the modified layer of high-k material is exposed to a wet etch fluid. The etch fluid may be an acid such as sulfuric acid. In step 706 the modified layer of high-k material is etched. When the process in step 706 has been carried out for the desired amount of time to etch the high-k layer, the

substrate is rinsed with deionized water and dried in step 708, and the process is ended in step 710.

**[0052]** The wet etching can be performed in a conventional cleaning or wet etching chamber, either operatively coupled to or within processing chamber 10.

**[0053]** The following examples are provided to further illustrate embodiments of the present invention and are not intended to restrict the scope of the invention.

**[0054]** EXAMPLE: Removal of a $HfO_2$ dielectric layer

**[0055]** A test structure was used that comprised patterned Si gate electrodes and a $HfO_2$ dielectric layer (50Å thick) overlying a Si substrate. In the absence of a plasma modifying step, the wet etch rate of the $HfO_2$ layer in hot sulfuric acid, was about 2-3A/hr. Removal of a $HfO_2$ layer that requires long wet etch runs, can introduce problems such as erosion of the interface between the $HfO_2$ layer and the gate electrode.

**[0056]** Alternatively, a plasma modifying step was performed on the above test structure in a capacitively coupled plasma process chamber, using a process gas comprising HBr and He gases. The substrate temperature was maintained at 80°C and the chamber pressure was 12mTorr. The test structure was exposed to the plasma for about 12sec, which resulted in a modified $HfO_2$ layer with a thickness of about 5A. Following the plasma process, the modified $HfO_2$ layer wet etched in hot sulfuric acid at a rate of about 2-3A/min, thereby showing greatly enhanced rate of removal when compared to a $HfO_2$ layer that was not subjected to the plasma modifying step. Furthermore, the wet etch step showed good selectivity of the $HfO_2$ dielectric layer to the source/drain regions.

**[0048]** In another example of the current invention, different plasma parameters were used plasma treat a $HfO_2$ layer, before wet etching the modified $HfO_2$ layer. The results are shown in Table I. In setup, a plasma was generated in the process chamber by RF powering the upper electrode and keeping the lower electrode at a floating potential by electrically insulating the lower electrode from the processing system. In this setup, a floating potential created in the lower electrode is thought to induce a strong electronic

(E) field across the $HfO_2$ layer, thereby modifying the $HfO_2$ layer. We speculate that the $HfO_2$ layer is possibly modified by diffusion of electronegative species (e.g., O) from the $HfO_2$ layer to underlying Si substrate. In another setup, the plasma processing system was run in RIE mode, where a plasma was generated by RF powering the lower electrode while keeping the upper electrode at a floating potential.

**[0049]** Table I

| Run | d1 (Å) | $T_{ESC}$ (°C) | Upper/lower power (W) | P (mTorr) | Ar flow (sccm) | G (mm) | Time (sec) | d2 (Å) | d3 (Å) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 119 | 80 | 400/0 | 100 | 112 | 90 | 20 | 119.4 | 113.1 |
| 2 | 119 | 80 | 400/0 | 100 | 112 | 90 | 60 | 120.2 | 113.1 |
| 3 | 118 | 80 | 0/400 | 100 | 112 | 90 | 20 | 120.1 | 99.2 |
| 4 | 119 | 80 | 0/400 | 100 | 112 | 90 | 60 | 118.7 | 92.6 |
| 5 | 71.6 | 30 | 0/600 | 30 | 560 | 80 | 80 | 20.5 | 3.7 |
| 6 | 72.1 | 30 | 0/400 | 30 | 560 | 80 | 80 | 7.5 | 2.0 |

**[0050]** In Table I, d1 is the initial $HfO_2$ layer thickness, d2 is the thickness of the plasma treated $HfO_2$ layer, and d3 is the thickness of the remaining $HfO_2$ layer following the wet etch of the plasma treated $HfO_2$ layer. $T_{ESC}$ is the temperature of the electrostatic chuck upon which the wafer is positioned, Upper/lower power is the RF power applied to the upper and lower electrodes, respectively, P is the chamber pressure, and Ar flow is the flow of Ar gas in the process chamber during the plasma treatment. The Ar gas flow further comprised 10sccm of $CF_4$ in Runs 1 and 2, to keep the high-k surface clean from quartz contamination during the plasma treatment. In Table I, the spacing between the upper and lower electrodes is denoted by G, and Time is the length of the plasma treatment. The frequency for the RF bias on the upper electrode was 60MHz, and 13.56MHz on the lower electrode. The wet etch step was carried out in dilute HF.

**[0051]** In Runs 1 and 2, RF power was applied to the upper electrode but the lower electrode was at a floating potential. These process condition are thought to result in minor ion-bombardment of the high-k layer from the plasma environment, as seen by the lack of removal of the $HfO_2$ layer during the plasma treatment. However, the plasma treatment in Runs 1 and 2 is

thought to results in E-field damage that modifies the high-k layer, as evidenced by removal of about 6A (5%) of the $HfO_2$ layer during the wet etch step. The E-field damage to the $HfO_2$ layer appears to saturate, since the same wet etch behavior was observed for the 20sec and 60sec plasma treatment runs.

**[0052]** In Runs 3 and 4, the plasma treatment process was carried out in RIE mode, where power was applied to the lower electrode but the upper electrode was at a floating potential . These process conditions did not lead to significant removal of $HfO_2$ during the plasma treatment, but the runs of 20sec and 60sec, lead to removal of 19A and 26A of $HfO_2$, respectively, during the following wet etch step.

**[0053]** In Runs 5 and 6, the plasma treatment process was also run in RIE mode, but using a higher Ar gas flow than in Runs 3 and 4. The higher Ar gas flows lead to sputtering of the $HfO_2$ layer with a sputtering rate greater than about 200A during the plasma treatment. The remainder of the plasma treated $HfO_2$ layer was effectively removed during the wet etch step. The $HfO_2$ layer residual left on the wafer after the plasma treatment in Run 5 is thought to be Hf-rich, and therefore the true residual layer thickness d3 is expected to be less than the measured 7.5A.

**[0054]** Numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.